

**8-BIT MICROCOMPUTER**

ADVANCE DATA

**HARDWARE FEATURES**

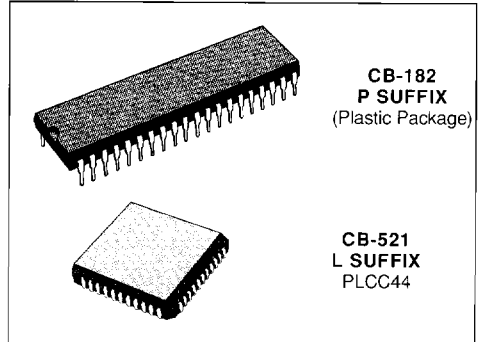
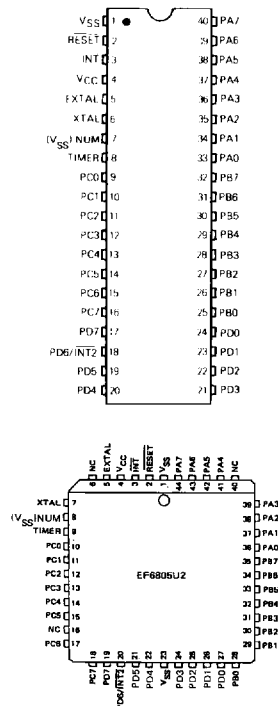
- 32 TTL/CMOS COMPATIBLE I/O LINES
- 24 BIDIRECTIONAL (8 lines are LED compatible)
- 8 INPUT-ONLY
- 2048 BYTES OF USER ROM
- 64 BYTES OF RAM
- SELF-CHECK MODE
- ZERO-CROSSING DETECT/INTERRUPT
- INTERNAL 8-BIT TIMER WITH 7-BIT MASK PROGRAMMABLE PRESCALER AND CLOCK SOURCE
- 5V SINGLE SUPPLY

**SOFTWARE FEATURES**

- 10 POWERFUL ADDRESSING MODES
- BYTE EFFICIENT INSTRUCTION SET WITH TRUE BIT MANIPULATION, BIT TEST, AND BRANCH INSTRUCTIONS
- SINGLE INSTRUCTION MEMORY EXAMINE/CHANGE
- POWERFUL INDEXED ADDRESSING FOR TABLES
- FULL SET OF CONDITIONAL BRANCHES
- MEMORY USABLE AS REGISTER/FLAGS
- COMPLETE DEVELOPMENT SYSTEM SUPPORT ON INICE®

**USER SELECTABLE OPTIONS**

- INTERNAL 8-BIT TIMER WITH SELECTABLE CLOCK SOURCE (External Timer Input or Internal Machine Clock)
- TIMER PRESCALER OPTION (7 Bits, 2<sup>n</sup>)
- 8 BIDIRECTIONAL I/O LINES WITH TTL OR TTL/CMOS INTERFACE OPTION
- 8 BIDIRECTIONAL I/O LINES WITH TTL OR OPEN-DRAIN INTERFACES OPTION
- CRYSTAL OR LOW-COST RESISTOR OSCILLATOR OPTION
- LOW VOLTAGE INHIBIT OPTION
- VECTORED INTERRUPTS TIMER, SOFTWARE, AND EXTERNAL
- USER CALLABLE SELF-CHECK SUBROUTINES


**PIN CONNECTION**


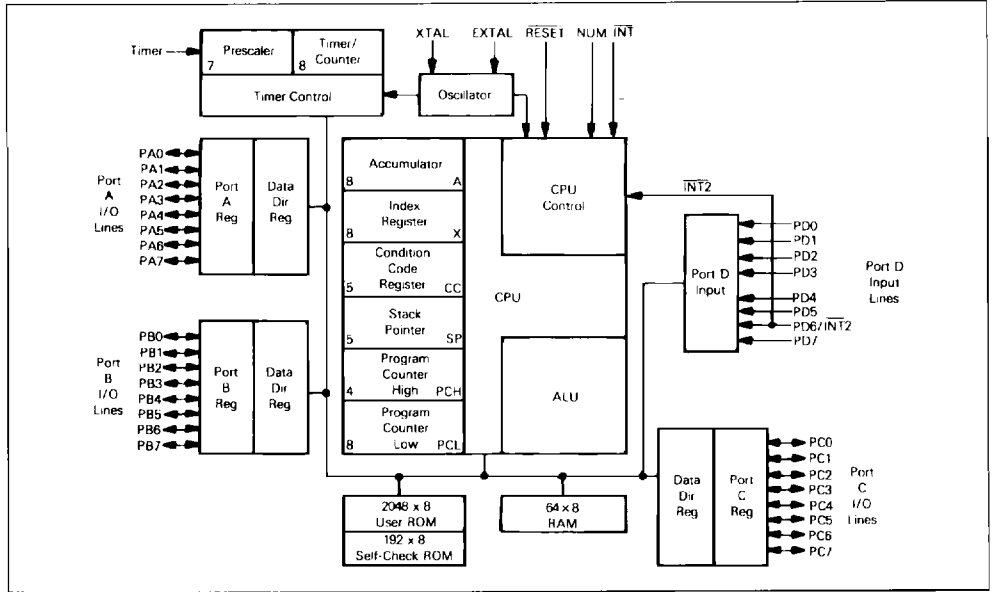
INICE® is SGS-THOMSON's development/emulation tool.

**DESCRIPTION**

The EF6805U2 Microcomputer Unit (MCU) is a member of the 6805 Family of low-cost single-chip Microcomputers. The 8-bit microcomputer contains a CPU, on-chip CLOCK, ROM, RAM, I/O, and

TIMER. It is designed for the user who needs an economical microcomputer with the proven capabilities of several members of the 6805 Family of microcomputers is shown at the end of this data sheet. The following are some of the hardware and software highlights of the EF6805U2 MCU.

**Figure 1 : EF6805U2 HMOS Microcomputer Block Diagram.**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	- 0.3 to + 7.0	V
V <sub>in</sub>	Input Voltage (except TIMER in self-check mode and open-drain inputs)	- 0.3 to + 7.0	V
V <sub>in</sub>	Input Voltage (open-drain pins, TIMER pin in self-check mode)	- 0.3 to + 15.0	V
T <sub>A</sub>	Operating Temperature Range (T <sub>L</sub> to T <sub>H</sub> )	0 to + 70 V Suffix - 40 to + 85 T Suffix - 40 to + 105	°C
T <sub>stg</sub>	Storage Temperature Range	- 55 to + 150	°C
T <sub>j</sub>	Junction Temperature	150	°C
	Plastic Package PLCC	150	

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V<sub>in</sub> and V<sub>out</sub> be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Reliability of operation is enhanced if unused inputs except EXTAL are tied to an appropriate logic voltage level (e.g. either V<sub>SS</sub> or V<sub>CC</sub>).

**THERMAL DATA**

θJA	Thermal Resistance	Plastic	50	°C/W
		PLCC	80	

## POWER CONSIDERATIONS

The average chip-junction temperature,  $T_J$ , in  $^{\circ}\text{C}$  can be obtained from :

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where :

$T_A$  = Ambient Temperature,  $^{\circ}\text{C}$

$\theta_{JA}$  = Package Thermal Resistance, Junction-to-Ambient,  $^{\circ}\text{C}/\text{W}$

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$ , Watts - Chip Internal Power

$P_{PORT}$  = Port Power Dissipation, Watts - User Determined

For most applications  $P_{PORT} \leq P_{INT}$  and can be neglected.  $P_{PORT}$  may become significant if the device

is configured to drive Darlington bases or sink LED loads.

An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{PORT}$  is neglected) is :

$$P_D = K + (T_J + 273^{\circ}\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives :

$$K = P_D \cdot (T_A + 273^{\circ}\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +5.25\text{Vdc} \pm 0.5\text{Vdc}$ ,  $V_{SS} = 0\text{Vdc}$ ,  $T_A = T_L$  to  $T_H$  unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH}$	Input High Voltage RESET ( $4.75 \leq V_{CC} \leq 5.75$ ) ( $V_{CC} < 4.75$ ) INT ( $4.75 \leq V_{CC} \leq 5.75$ ) ( $V_{CC} < 4.75$ ) All Other (except timer)	4.0 $V_{CC} - 0.5$ 4.0 $V_{CC} - 0.5$ 2.0		$V_{CC}$ $V_{CC}$ $V_{CC}$ $V_{CC}$ $V_{CC}$	V
$V_{IH}$	Input High Voltage Timer Timer Mode Self-check Mode	2.0 9.0	10.0	$V_{CC} + 1.0$ 15.0	V
$V_{IL}$	Input Low Voltage RESET INT All Other	$V_{SS}$ $V_{SS}$ $V_{SS}$		0.8 1.5 0.8	V
$V_{IRES+}$ $V_{IRES-}$	RESET Hysteresis Voltages (see figures 10, 11 and 12) "Out of Reset" "Into Reset"	2.1 0.8		4.0 2.0	V
$V_{INT}$	INT Zero Crossing Input Voltage, Through a Capacitor	2		4	$V_{ac\ p-p}$
$P_D$	Power Dissipation - (no port loading, $V_{CC} = 5.75\text{V}$ ) $T_A = 0^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$		520 580	740 800	mW
$C_{in}$	Input Capacitance EXTAL All Other		25 10		pF
$V_{LVR}$	Low Voltage Recover			4.75	V
$V_{LVI}$	Low Voltage Inhibit	2.75	3.75	4.70	V
$I_{in}$	Input Current TIMER ( $V_{in} = 0.4\text{V}$ ) INT ( $V_{in} = 2.4\text{V}$ to $V_{CC}$ ) EXTAL ( $V_{in} = 2.4\text{V}$ to $V_{CC}$ - crystal option) ( $V_{in} = 0.4\text{V}$ - crystal option) RESET ( $V_{in} = 0.8\text{V}$ ) - External Capacitor Charging Current	-40.0	20	20 50 10 -1600 -40	$\mu\text{A}$

\* Due to internal biasing this input (when unused) floats to approximately 2.2V.

**SWITCHING CHARACTERISTICS**

( $V_{CC} = + 5.25Vdc \pm 0.5Vdc$ ,  $V_{SS} = 0Vdc$ ,  $T_A = T_L$  to  $T_H$  unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$f_{osc}$	Oscillator Frequency	0.4		4.2	MHz
$t_{cyc}$	Cycle Time ( $4/f_{osc}$ )	0.95		10	$\mu s$
$t_{WL}, t_{WH}$	INT, INT2, and TIMER Pulse Width (see interrupt section)	$t_{cyc} + 250$			ns
$t_{RWL}$	RESET Pulse Width	$t_{cyc} + 250$			ns
$f_{INT}$	INT Zero-crossing Detection Input Frequency	0.03		1	kHz
	External Clock Input Duty Cycle (EXTAL)	40	50	60	%
	Crystal Oscillator Start-up Time*			100	ms

\* See figure 16 for typical crystal parameters.

**PORT ELECTRICAL CHARACTERISTICS**

( $V_{CC} = + 5.25Vdc \pm 0.5Vdc$ ,  $V_{SS} = 0Vdc$ ,  $T_A = T_L$  to  $T_H$  unless otherwise noted)

**PORT A WITH CMOS DRIVE ENABLED**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{OL}$	Output Low Voltage ( $I_{Load} = 1.6mA$ )			0.4	V
$V_{OH}$	Output High Voltage $I_{Load} = - 100\mu A$ $I_{Load} = - 10\mu A$	2.4 $V_{CC} - 1.0$			V
$V_{IH}$	Input High Voltage ( $I_{Load} = - 300\mu A$ max.)	2.0		$V_{CC}$	V
$V_{IL}$	Input Low Voltage ( $I_{Load} = - 500\mu s$ max.)	$V_{SS}$		0.8	V
$I_{IH}$	High Z State Input Current ( $V_{in} = 2.0V$ to $V_{CC}$ )			- 300	$\mu A$
$I_{IL}$	High Z State Input Current ( $V_{in} = 0.4V$ )			- 500	$\mu A$

**PORT B**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{OL}$	Output Low Voltage $I_{Load} = 3.2mA$ $I_{Load} = 10mA$ (sink)			0.4 1.0	V
$V_{OH}$	Output High Voltage $I_{Load} = - 200\mu A$	2.4			V
$I_{OH}$	Darlington Current Drive (source) $V_O = 1.5V$	- 1.0		- 10	mA
$V_{IH}$	Input High Voltage	2.0		$V_{CC}$	V
$V_{IL}$	Input Low Voltage	$V_{SS}$		0.8	V
$I_{TSI}$	High Z State Input Current		< 2	10	$\mu A$

**PORT C AND PORT A WITH CMOS DRIVE DISABLED**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{OL}$	Output Low Voltage $I_{Load} = 1.6mA$			0.4	V
$V_{OH}$	Output High Voltage $I_{Load} = - 100\mu A$	2.4			V
$V_{IH}$	Input High Voltage	2.0		$V_{CC}$	V
$V_{IL}$	Input Low Voltage	$V_{SS}$		0.8	V
$I_{TSI}$	High Z State Input Current		< 2	10	$\mu s$

**PORT ELECTRICAL CHARACTERISTICS** (continued)

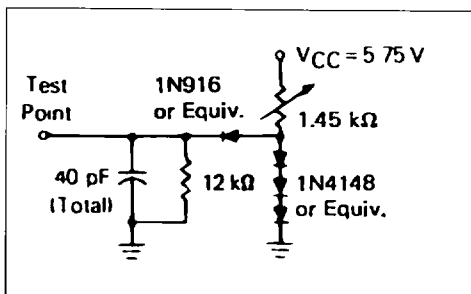
PORT C (open-drain option)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	2.0		13.0	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub>		0.8	V
I <sub>LOD</sub>	Input Leakage Current		< 3	15	μA
V <sub>OL</sub>	Output Low Voltage I <sub>L,load</sub> = 1.6mA			0.4	V

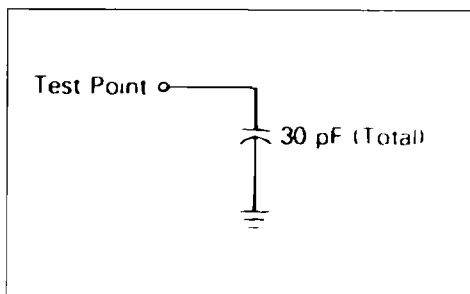
PORT D

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	2.0		V <sub>CC</sub>	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub>		0.8	V
I <sub>in</sub>	Input Current		< 1	5	μA

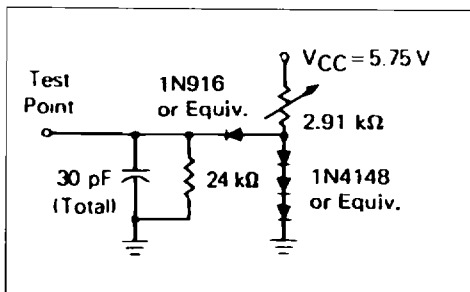
**Figure 2 :** TTL Equivalent Test Load (port B).



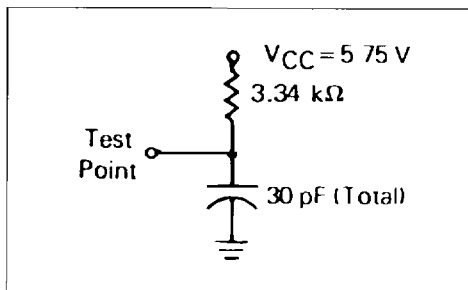
**Figure 3 :** CMOS Equivalent Test Load (port A).



**Figure 4 :** TTL Equivalent Test Load (ports A and C).



**Figure 5 :** Open-drain Equivalent Test Load (port C).



**SIGNAL DESCRIPTION**

The input and output signals for the MCU, shown in figure 1, are described in the following paragraphs.

**V<sub>CC</sub> AND V<sub>SS</sub>** - Power is supplied to the MCU using these two pins. V<sub>CC</sub> is power and V<sub>SS</sub> is the ground connection.

**INT** - This pin provides the capability for asynchronously applying an external interrupt to the MCU.

Refer to Interrupts Section for additional information.

**XTAL AND EXTAL** - These pins provide control input for the on-chip clock oscillator circuit. A crystal, a resistor, or an external signal, depending on user selectable manufacturing mask option, can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins

should be minimized. Refer to Internal Clock Generator Options Section for recommendations about these inputs.

NUM (NON USER MODE) - This pin is not for user application and must be connected to V<sub>SS</sub>.

TIMER - The pin allows an external input to be used to control the internal timer circuitry and also to initiate the self test program. Refer to Timer Selection for additional information about the timer circuitry.

RESET - This pin allows resetting of the MCU at times other than the automatic resetting capability already in the MCU. The MCU can be reset by pulling RESET low. Refer to Resets Section for additional information.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7) - These 32 lines are arranged into four 8-bit ports (A, B, C, and D). Ports A, B, and C are programmable as either inputs or outputs under software control of the data direction registers (DDRs). Port D is for digital input only and bit 6 may be used for a second interrupt INT2. Refer to Input/Output Section and Interrupts Section for additional information.

MEMORY - The MCU is capable of addressing 4096 bytes of memory and I/O registers with its program counter. The EF6805U2 MCU has implemented 2314 of these bytes. This consists of 2048 user ROM bytes, 192 self-check ROM bytes, 64 user RAM bytes, 7 port I/O bytes, 2 timer registers, and a miscellaneous register ; see figure 6 for the Address map. The user ROM has been split into three areas. The main user ROM area is from \$080 to \$0FF and from \$7C0 to \$F37. The last 8 user ROM locations at the bottom of memory are for the interrupt vectors.

The MCU reserves the first 16 memory locations for I/O features, of which 10 have been implemented. These locations are used for the ports, the port DDRs, the timer and the INT2 miscellaneous register, and the 64 RAM bytes, 31 bytes are shared with the stack area. The stack must be used with care when data shares the stack area.

The shared stack area is used during the processing of an interrupt or subroutine calls to save the contents of the CPU state. The register contents are pushed onto the stack in the order shown in figure 7. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program.

Figure 6 : EF6805U2 MCU Address Map.

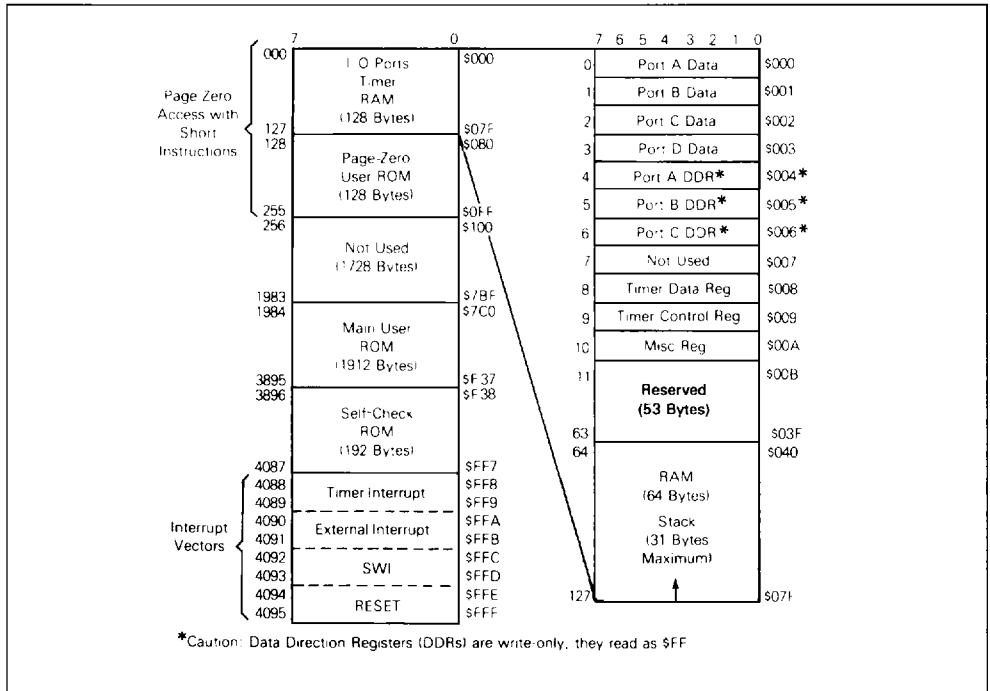
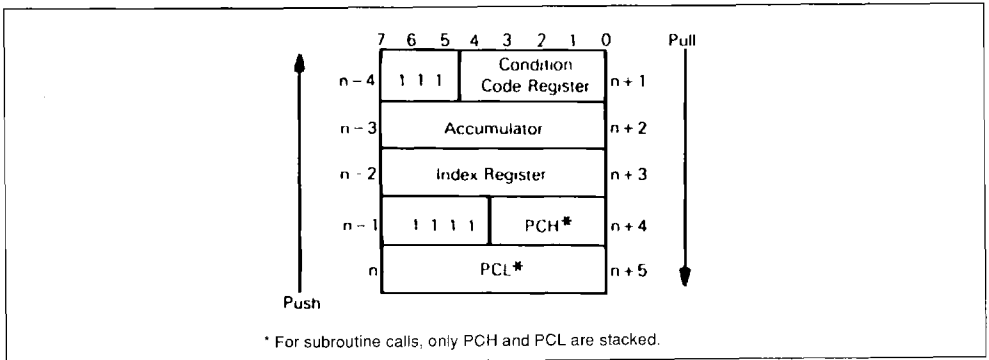


Figure 7 : Interrupt Stacking Order.



**CENTRAL PROCESSING UNIT**

The CPU of the EF6805 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal address, data, and control buses.

**REGISTERS**

The 6805 Family CPU has five registers available to the programmer. They are shown in figure 8 and are explained in the following paragraphs.

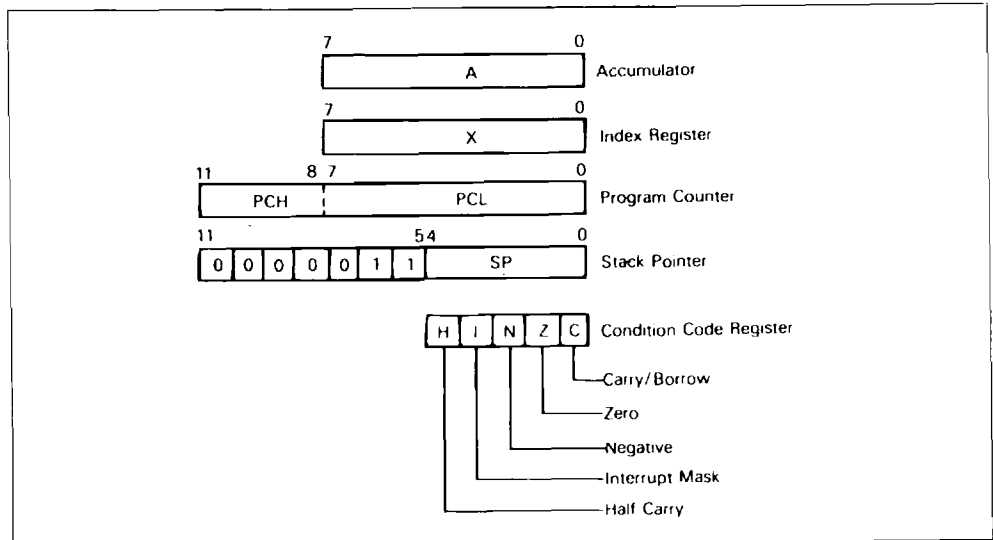
**ACCUMULATOR (A)** - The accumulator is a general purpose 8-bit register used to hold operands and re-

sults of arithmetic calculations or data manipulations.

**INDEX REGISTER (X)** - The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit value that may be added to an instruction value to create an effective address. The index register can also be used for data manipulations using the read-modify-write instructions. The Index Register may also be used as a temporary storage area.

**PROGRAM COUNTER (PC)** - The Program Counter is a 12 bit register that contains the address of the next instruction to be executed.

Figure 8 : Programming Model.



**STACK POINTER (SP)** - The stack pointer is a 12-bit register that contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location \$07F. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is then pulled from the stack. The seven most significant bits of the stack pointer are permanently set to 000011. Subroutines and interrupts may be nested down to location \$061 (31 bytes maximum) which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).

**CONDITION CODE REGISTER (CC)** - The condition code register is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

**Half Carry (H)** - Set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

**Interrupt (I)** - When this bit is set, the timer and external interrupts (INT and INT2) are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

**Negative (N)** - When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical "1").

**Zero (Z)** - When set, this bit indicates that the result of the last arithmetic, or data manipulation was zero.

**Carry/Borrow (C)** - When set, this bit indicates that a carry or borrow out of the Arithmetic Logic Unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions plus shifts and rotates.

## TIMER

The timer circuitry for the MC6805U2 is shown in figure 10. The 8-bit counter may be loaded under program control and is decremented toward zero by the clock input (or prescaler output). When the timer reaches zero, the timer interrupt request bit (bit 7) in the timer control register (TCR) is set. The timer interrupt can be masked (disabled) by setting the timer interrupt mask bit (bit 6) in the TCR. The interrupt bit (I bit) in the condition code register also prevents a timer interrupt from being processed. The

MCU responds to this interrupt by saving the present CPU state on the stack, fetching the timer interrupt vector from locations \$FF8 and \$FF9 and executing the interrupt routine (see **RESET, CLOCK, AND INTERRUPT STRUCTURE SECTIONS**). The timer interrupt request bit must be cleared by software. The interrupt request bit must be cleared by software. The TIMER and INT2 share the same interrupt vector. The interrupt routine must check the request bits to determine the source of the interrupt.

The clock input to the timer can be from an external source (decrementing of timer counter occurs on a positive transition of the external source) applied to the TIMER input pin, or it can be the internal phase two signal. Three machine cycles are required for a change in state of the TIMER pin to decrement the timer prescaler. The maximum frequency of a signal that can be recognized by the TIMER pin logic is dependent on the parameter labeled  $t_{WH}$ . The pin logic that recognizes the high state on the pin must also recognize the low state on the pin in order to "re-arm" the internal logic. Therefore, the period can be calculated as follows (assumes 50/50 duty cycle for a given period) :

$$t_{cyc} \times 2 + 250ns = \text{period} = \frac{1}{\text{freq}}$$

The periods is not simply  $t_{WH} + t_{WL}$ . This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily longer period (250 nanoseconds times two).

When the phase two signal is used as the source, it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the mask options that is specified before manufacture of the MCU.

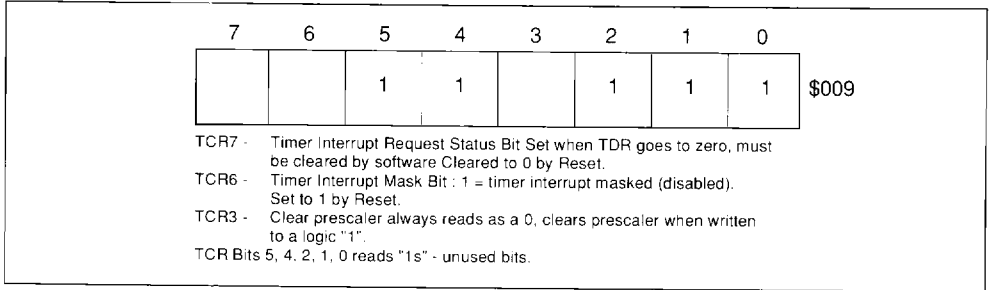
## NOTE

For ungated phase two clock input to the timer prescaler, the TIMER pin should be tied to  $V_{CC}$ .

A prescaler option, divide by  $2^n$ , can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling mask option is also specified before manufacture. To avoid truncation errors, the prescaler is cleared when bit 3 of the timer control register is written to a logic one (this bit always reads a logic zero). See figure 9.



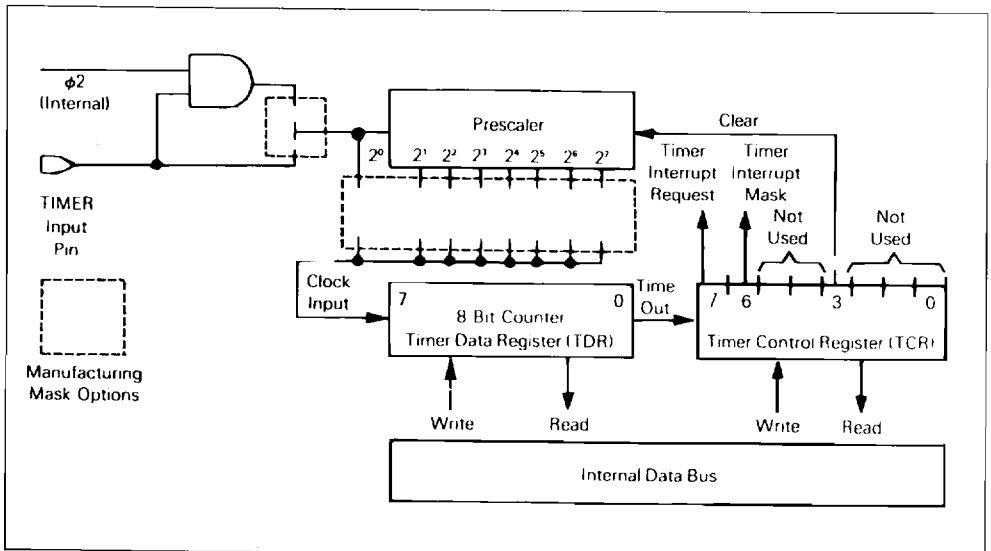
Figure 9 : Timer Control Register (TCR).



The timer continues to count past zero, falling through to \$FF from \$00 and then continuing the count down. Thus the counter can be read at any time by reading the timer data register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred, and not disturb the counting process.

At power up or reset, the prescaler and counter are initialized with all logic ones ; the timer interrupt request bit (bit 7) is cleared and the timer interrupt mask bit (bit 6) is set.

Figure 10 : Timer Block Diagram.



### SELF-CHECK

The self-check capability of the EF6805U2MCU provides an internal check to determine if the part is functional. Connect the MCU as shown in Figure 11 and monitor the output of Port C bit 3 for an oscillation of approximately 7Hz. A 10-volt level (through a 10k resistor) on the timer input, pin 8 and pressing then releasing the RESET button, energizes the ROM-based self-check feature. The self-check pro-

gram exercises the RAM, ROM, TIMER, interrupts, and I/O ports.

Several of the self-check subroutines can be called by a user program with a JSR or BSR instruction. They are the RAM, ROM, tests. The timer routine may also be called if the timer input is the internal  $\phi 2$  clock.

To call those subroutines in customer applications, please contact your SGS-THOMSON Microelectro-

nics sales office in order to obtain the complete description of the self-check program and the entrance/exit conditions.

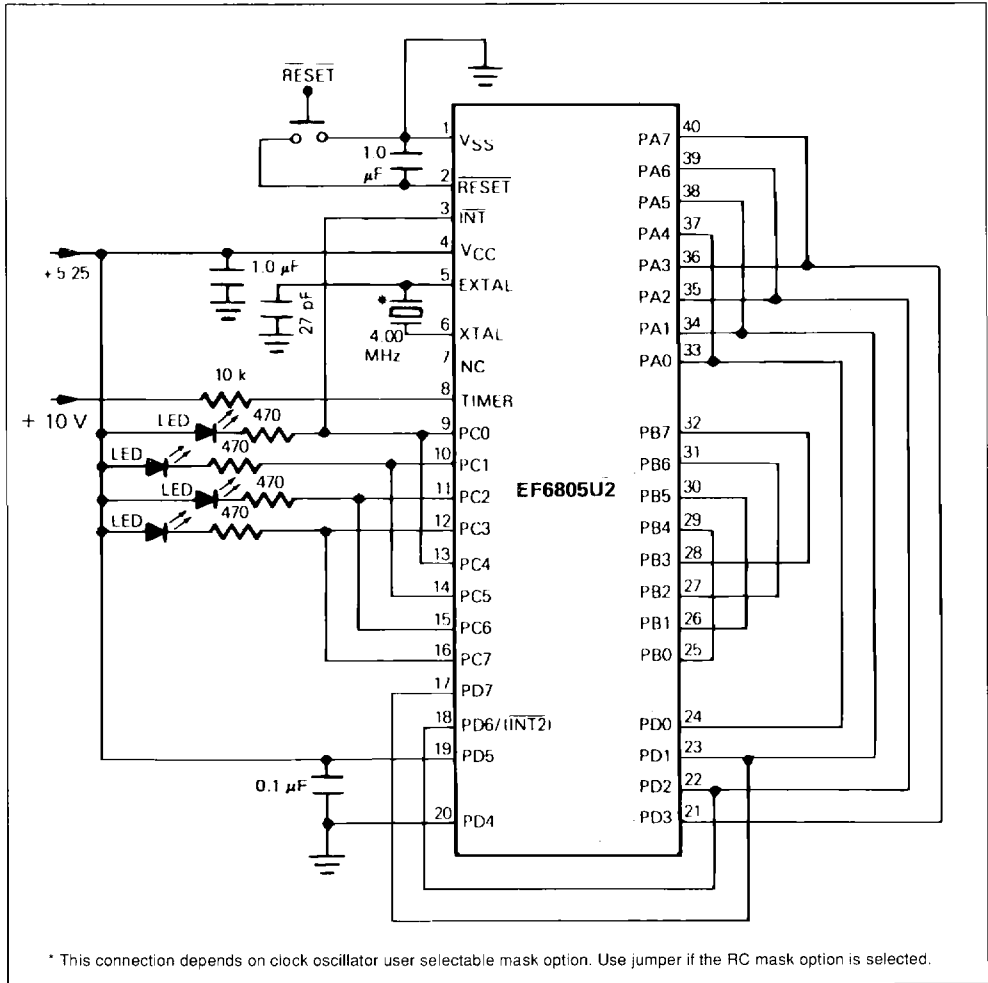
**RAM SELF-CHECK SUBROUTINE** - The RAM self-check is called at location \$F6F and returns with the Z bit clear if any error is detected ; otherwise the Z bit is set. The walking diagnostic pattern method is used on the EF6805U2.

The RAM test must be called with the stack pointer at \$07F. When run, the test checks every RAM cell except for \$07F and \$07E which are assumed to contain the return address.

The A and X registers and all RAM locations except \$07F and \$07E are modified.

**ROM CHECKSUM SUBROUTINE** - The ROM self-check is called at location \$F8A. If any error is detected, it returns with the Z bit cleared ; otherwise Z = 1, X = 0 on return, and A is zero if the test passes. RAM location \$040 to \$043 is overwritten. The checksum is the complement of the execution OR of the contents of the user ROM.

Figure 11 : Self-check connections.



**LED MEANINGS**

PC0	PC1	PC2	PC3	Remarks (1 : LED ON ; 0 : LED OFF)
1	0	1	0	Bad I/O
0	0	1	0	Bad Timer
1	1	0	0	Bad RAM
0	1	0	0	Bad ROM
0	0	0	0	Bad Interrupts or Request Flag
All Flashing				Good Device

**Note :** Anything else bord Device, bad Port C, etc.

**TIMER SELF-CHECK SUBROUTINE** - The timer self-check is called at location \$FCF and returns with the Z bit cleared if any error was found ; otherwise Z = 1.

In order to work correctly as a user subroutine, the internal  $\emptyset 2$  clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock is running and the interrupt mask is not set so the caller must protect from interrupts if necessary.

The A and X register contents are lost. The timer self-check routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of 2 since the prescaler is a power of 2. If not, the timer is probably not counting correctly. The routine also detects a timer which is not running.

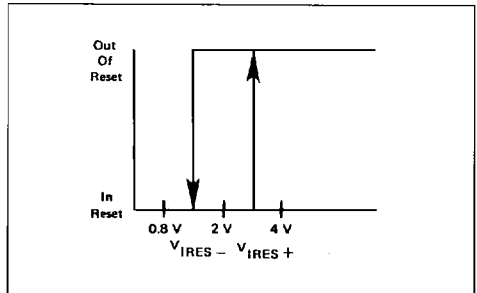
**RESET**

The MCU can be reset three ways : by initial power-up, by the external reset input (RESET) and by an

optional internal low-voltage detect circuit. The RESET input consists mainly of a Schmitt trigger which senses the RESET line logic level. A typical reset Schmitt trigger hysteresis curve is shown in figure 12. The Schmitt trigger provides an internal reset voltage if it senses a logical zero on the RESET pin.

**Power-On Reset (POR)** - An internal reset is generated upon powerup that allows the internal clock generator to stabilize. A delay of  $t_{RHL}$  milliseconds is required before allowing the RESET input to go high. Refer to the power and reset timing diagram of figure 13. Connecting a capacitor to the RESET input (as illustrated in figure 14) typically provides sufficient delay. During poerup, the Schmitt trigger switches on (remove reset) when RESET rises to  $V_{IRES+}$ .

**Figure 12 :** Typical Reset Schmitt Trigger Hysteresis



**Figure 13 :** Power and Reset Timing.

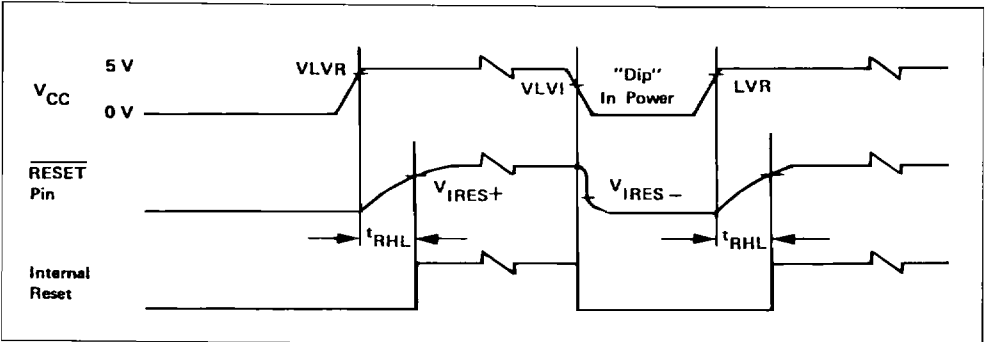
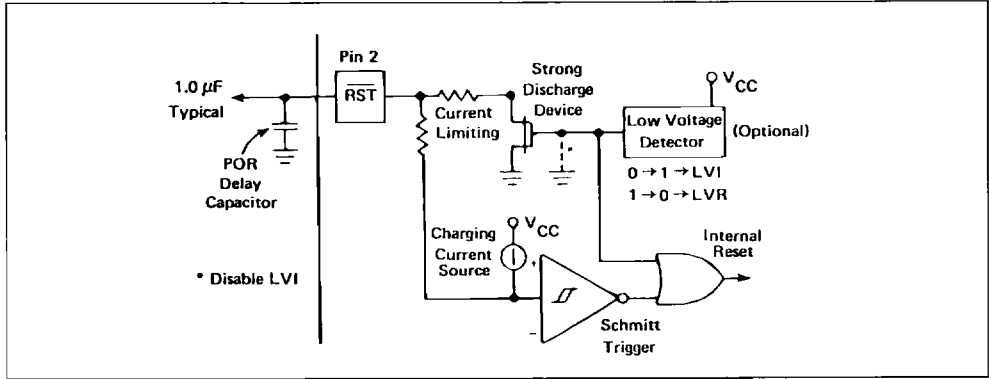


Figure 14 :  $\overline{\text{RESET}}$  Configuration.



**External Reset Input** - The MCU will be reset if a logical zero is applied to the  $\overline{\text{RESET}}$  input for a period longer than one machine cycle ( $t_{\text{cyc}}$ ). Under this type of reset, the Schmitt trigger switches off at  $V_{\text{IRES}}$  to provide an internal voltage.

**Low-voltage Inhibit (LVI)** - The optional low-voltage detection circuit causes a reset of the MCU if the power supply voltage falls below a certain level ( $V_{\text{LVI}}$ ). The only requirement is that  $V_{\text{CC}}$  remains at or below the  $V_{\text{LVI}}$  threshold for one  $t_{\text{cyc}}$  minimum. In typical applications, the  $V_{\text{CC}}$  bus filter capacitor will eliminate negative-going voltage glitches of less than one  $t_{\text{cyc}}$ . The output from the low voltage detector is connected directly to the internal reset circuitry. It also forces the  $\overline{\text{RESET}}$  pin low via a strong discharge device through a resistor. The internal reset will be removed once the power supply voltage rises above a recovery level ( $V_{\text{LVR}}$ ), at which time a normal power-on-reset occurs.

**INTERNAL CLOCK GENERATOR OPTIONS**

The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor, a jumper wire, or an external signal may be used to generate a system clock with various stability/cost trade-offs. The oscillator frequency is internally divided by four to produce the internal system clocks. A manufacturing mask option is used to select crystal or resistor operation.

The different connection methods are shown in

figure 15. Crystal specifications and suggested PC board layouts are given in figure 16. A resistor selection graph is given in figure 17.

The crystal oscillator start-up time is a function of many variables: crystal parameters (especially  $R_s$ ), oscillator load capacitances, IC parameters, ambient temperature, and supply voltage. To ensure rapid oscillator start up, neither the crystal characteristics nor the load capacitances should exceed recommendations.

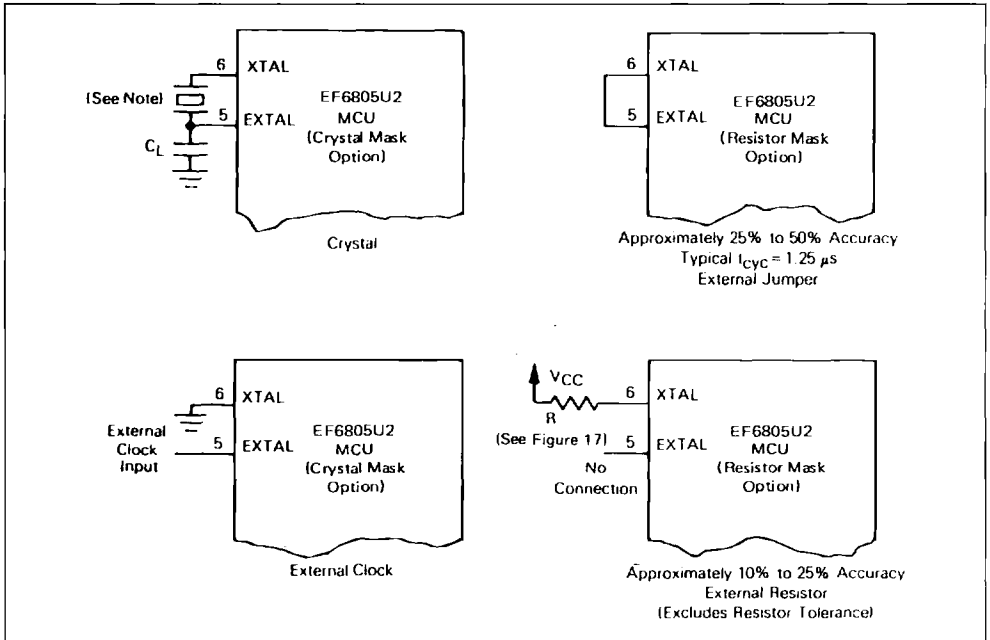
When utilizing the on-board oscillator, the MCU should remain in a reset condition (reset pin voltage below  $V_{\text{IRES+}}$ ) until the oscillator has stabilized at its operating frequency. Several factors are involved in calculating the external reset capacitor required to satisfy this condition: the oscillator start-up voltage, the oscillator stabilization time, the minimum  $V_{\text{IRES+}}$ , and the reset charging current specification.

Once  $V_{\text{CC}}$  minimum is reached, the external  $\overline{\text{RESET}}$  capacitor will begin to charge at a rate dependent on the capacitor value. The charging current is supplied from  $V_{\text{CC}}$  through a large resistor, so it appears almost like a constant current source until the reset voltage rises above  $V_{\text{IRES+}}$ . Therefore, the  $\overline{\text{RESET}}$  pin will charge at approximately:

$$(V_{\text{IRES+}}) \cdot C_{\text{ext}} = I_{\text{RES}} \cdot t_{\text{RHL}}$$

Assuming the external capacitor is initially discharged.

Figure 15 : Clock Generator Options.



**Note :** The recommended  $C_L$  value with a 4.0MHz crystal is 27pF maximum, including system distributed capacitance. There is an internal capacitance of approximately 25pF on the XTAL pin. For crystal frequencies other than 4MHz, the total capacitance on each pin should be scaled as the inverse of the frequency ratio. For example, with a 2MHz crystal, use approximately 50pF on EXTAL and approximately 25pF on XTAL. The exact value depends on the Motional-Arm parameters of the crystal used.

Figure 16 : Crystal Motional ARM Parameters and Suggested PC Board Layout.

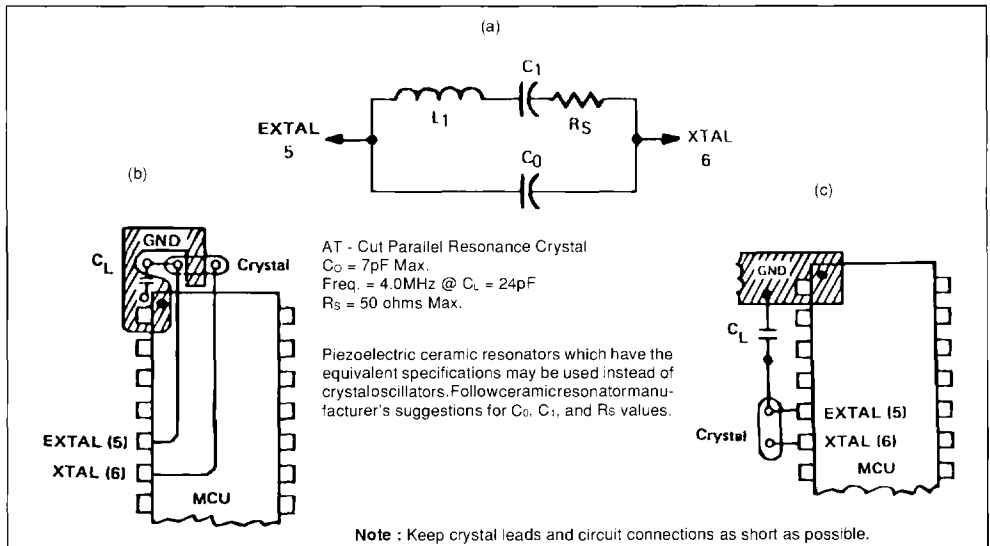
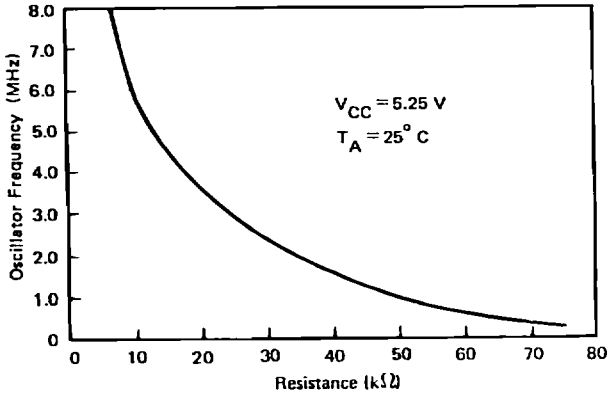


Figure 17 : Typical Frequency Selection for Resistor (oscillator option).



## INTERRUPTS

The microcomputers can be interrupted four different ways : through the external interrupt (INT) input pin, the internal timer interrupt request, the external port D bit 6 ( $\overline{\text{INT2}}$ ) input pin, or the software interrupt instruction (SWI). When any interrupt occurs : the current instruction (including SWI) is completed, processing is suspended, the present CPU state is pushed onto the stack, the interrupt bit (1) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. Stacking the CPU register, setting the I bit, and vector fetching require a total of 11  $t_{\text{cyc}}$  periods for completion. A flowchart of the interrupt sequence is shown in figure 18. The interrupt service routine must end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt (by unstacking the previous CPU state). Unlike RESET, hardware interrupts do not cause the current ins-

truction execution to be halted, but are considered pending until the current instruction execution is complete.

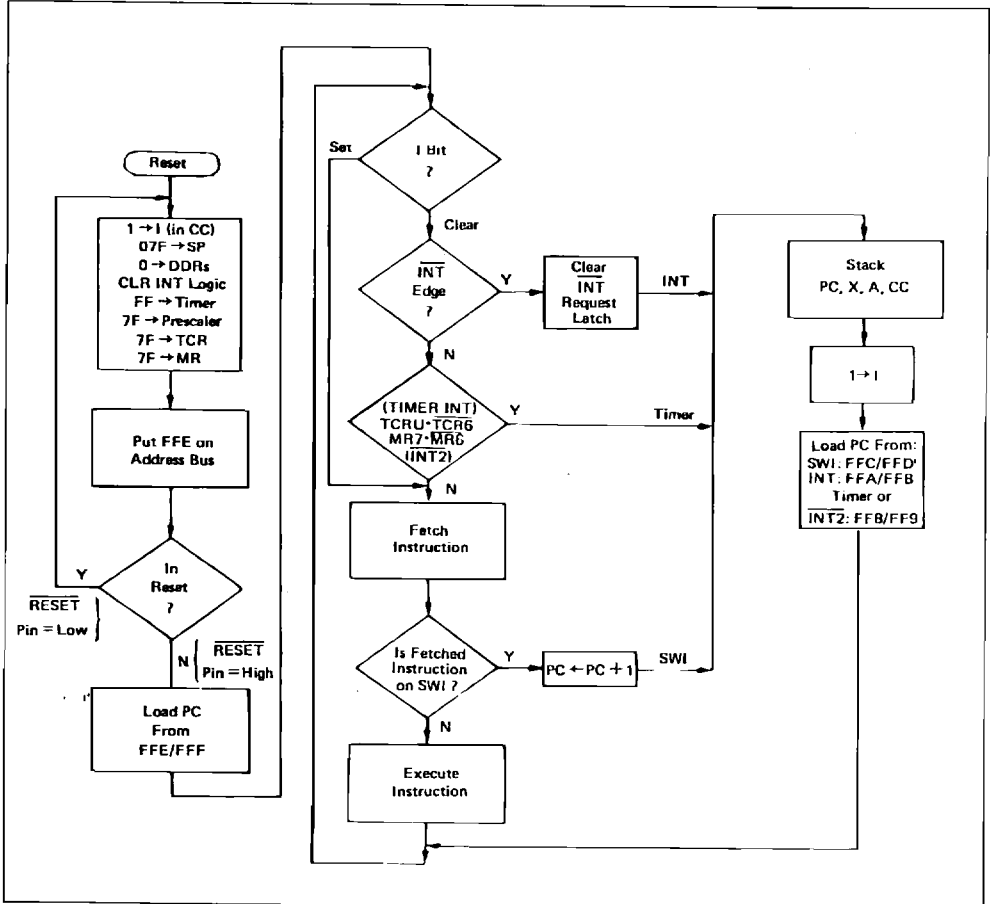
When the current instruction is complete, the processor checks all pending hardware interrupts and if unmasked, proceeds with interrupt processing ; otherwise the next instruction is fetched and executed. Note that masked interrupts are latched for later interrupt service.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed as any other instruction.

## NOTE

The timer and  $\overline{\text{INT2}}$  interrupts share the same vector address. The interrupt routine must determine the source by examining the interrupt request bits (TCR b7 and MR b7). Both b7 and MR b7 can only be written to zero by software.

Figure 18 : Reset and Interrupt Processing Flowchart.



The external interrupt,  $\overline{\text{INT}}$  and  $\overline{\text{INT2}}$ , are synchronized and then latched on the falling edge of the input signal. The  $\overline{\text{INT2}}$  interrupt has an interrupt request bit (bit 7) and a mask bit (bit 6) located in the miscellaneous register (MR). The  $\overline{\text{INT2}}$  interrupt is inhibited when the mask bit is set. The  $\overline{\text{INT2}}$  is always read as a digital input on port D. The  $\overline{\text{INT2}}$  and timer interrupt request bits, if set, cause the MCU to process an interrupt when the condition code I bit is clear.

A sinusoidal input signal ( $f_{\text{INT}}$  maximum) can be used to generate an external interrupt for use as a zero-crossing detector. This allows applications such as servicing time-of-day routines and engag-

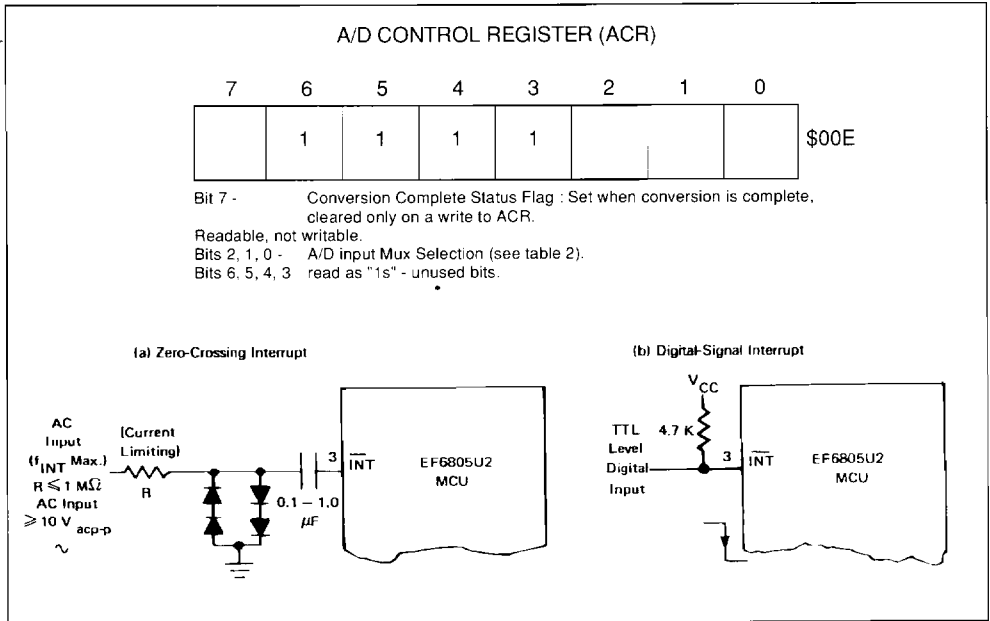
ing/disengaging ac power control devices. Off-chip full wave rectification provides an interrupt at every zero crossing of the ac signal and thereby provides a 2f clock. See figure 19.

#### NOTE

The  $\overline{\text{INT}}$  (pin 3) is internally biased at approximately 2.2V due to the internal zero-crossing detection.

A software interrupt (SWI) is an executable instruction which is executed regardless of the state of the I bit in the condition code register. SWIs are usually used as break-points for debugging or as systems calls.

Figure 19 : Typical Interrupt Circuits.



INPUT/OUTPUT CIRCUITRY

There are 32 input/output pins. The  $\overline{INT}$  pin may be polled with branch instructions to provide an additional input pin. All pins on ports A, B, and C are programmable as either inputs or outputs under software control of the corresponding data direction register (DDR). See below I/O port control registers configuration. The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output or a logic zero for input. On reset all the DDRs are initialized to a logic zero state, placing the ports in the input mode.

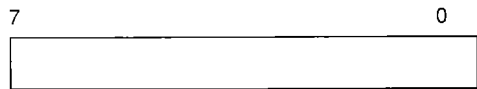
The port output registers are not initialized on reset and should be initialized by software before changing the DDRs from input to output. A read operation on a port programmed as an output will read the contents of the output latch regardless of the logic levels at the output pin, due to output loading. Refer to figure 20.

PORT DATA REGISTER



Port A Addr = \$000  
 Port B Addr = \$001  
 Port C Addr = \$002  
 Port D Addr = \$003

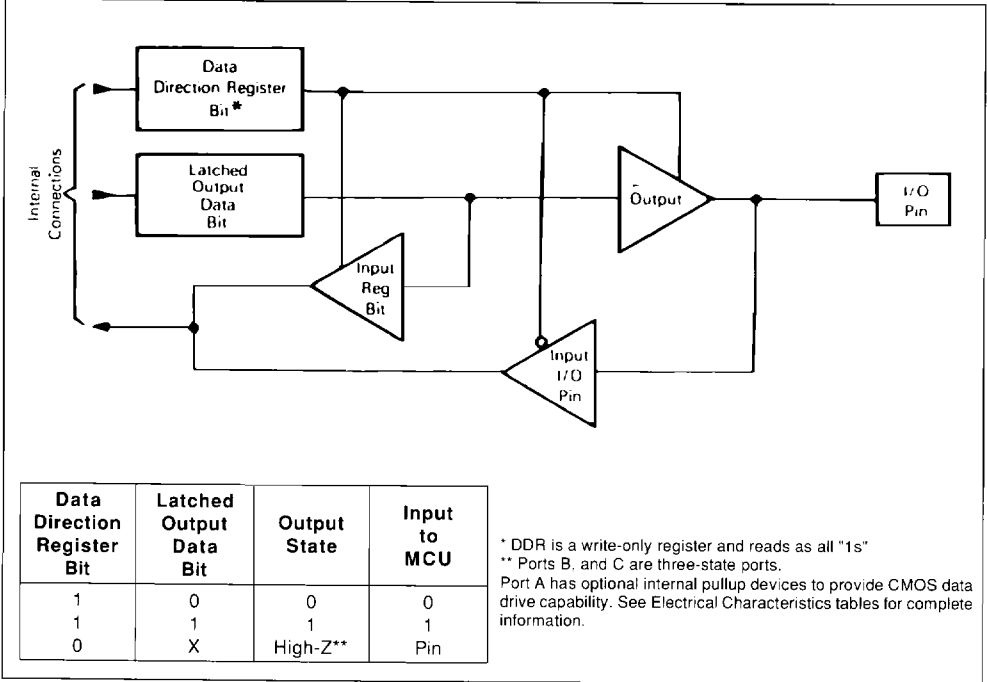
PORT DATA DIRECTION REGISTER (DDR)



- (1) Write only ; reads as all "1s"
- (2) 1 = Output, 0 = Input Cleared to 0 by Reset
- (3) Port A Addr = \$004  
Port B Addr = \$005  
Port C Addr = \$006



Figure 20 : Typical Port I/O Circuitry.



All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs (mask option) while port B, C, and D lines are CMOS compatible as inputs. Port D lines are input only ; thus, there is no corresponding DDR. When programmed as outputs, port B is capable of sinking 10 milliamperes and sourcing 1 milliampere on each pin.

The address map (figure 6) gives the addresses of data registers and data direction registers. Figure 21 provides some examples of port connections.

**CAUTION**

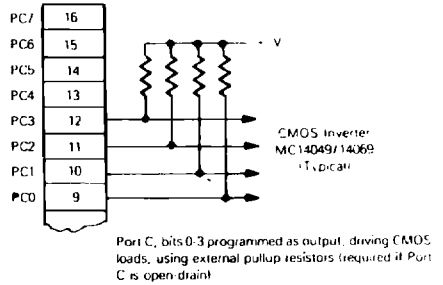
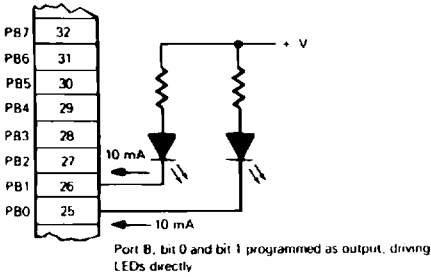
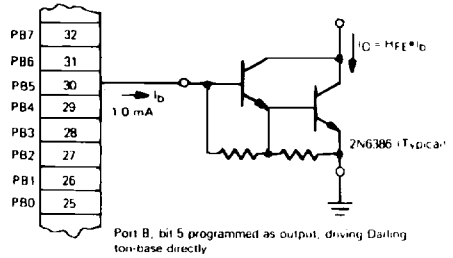
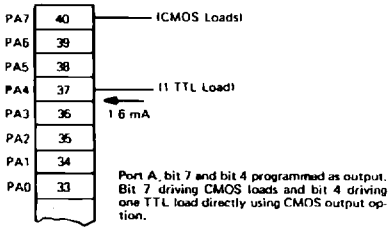
The corresponding DDRs for ports A, B, and C are write-only registers (registers at \$004, \$005, \$006). A read operation on these registers is undefined

Since BSET and BCLR are read-modify write in function, they cannot be used to clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be written using a single-store instruction.

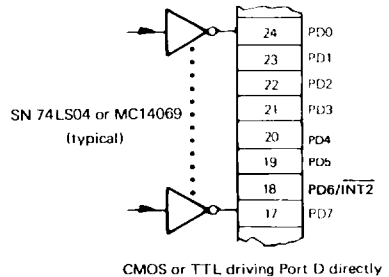
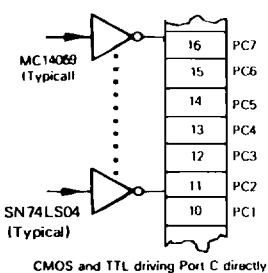
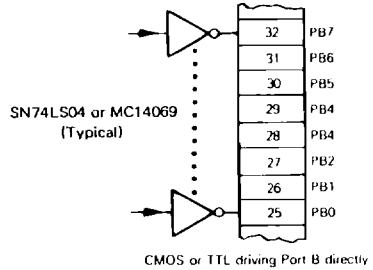
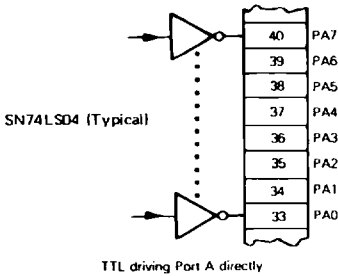
The latched output data bit (see figure 20) must always be written. Therefore, any write to a port writes all of its data bits even though the port DDR is set to input. This may be used to initialize the data register and avoid undefined outputs ; however, care must be exercised when using read-modify-write instructions, since the data read corresponds to the pin level if the DDR is an input (zero) and corresponds to the latched output data when the DDR is an output (one).

Figure 21 : Typical Port Connections.

(a) Output Modes



(b) Input Modes



## BIT MANIPULATION

The EF6805U2 has the ability to set or clear a single RAM or I/O bit (except the data direction registers) with a single instruction (BSET, BCLR) (see Caution below). Any bit in page zero can be tested using the BRSET and BRCLR instructions and the program branches as a result of its state. The carry bit equals the value of the bit references by BRSET or BRCLR. The capability to working with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines.

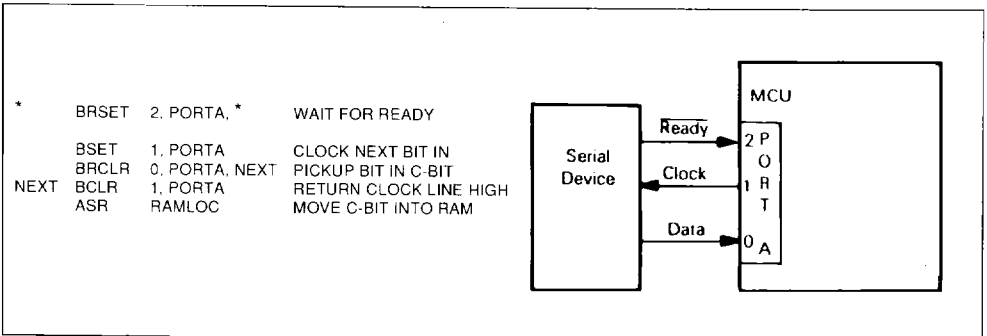
### CAUTION

The corresponding data direction registers for ports A, B, and C are write-only registers (locations \$004, \$005, and \$006). A read operation on these regis-

ters is undefined. Since BSET and BCLR are read-modify-write functions, they cannot be used to set a data direction register bit (all "unaffected" bits would be set). It is recommended that all data direction register bits in a port be written using a single-store instruction.

The coding examples shown in figure 22 illustrates the usefulness of the bit manipulation and test instruction. Assume that the microcomputer is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line to clock data one bit at a time, least significant bit first out of the device. The microcomputer waits until the data is ready, clocks the external device, picks up the data in the carry flag, clears the clock line, and finally accumulates the data bit in a random-access memory location.

Figure 22 : Bit Manipulation Example.



## ADDRESSING MODES

The EF6805U2 MCU has ten addressing modes available for use by the programmer. They are explained briefly in the following paragraphs. For additional details and graphical illustrations, refer to the EF6805 Family Users Manual.

The term "effective address" (EA) is used in describing the addressing modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

**Immediate** - In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

**Direct** - In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in

memory with a single 2-byte instruction. This address area includes all on-chip RAM and I/O registers and 128 bytes of ROM. Direct addressing is an effective use of both memory and time.

**Extended** - In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single 3-byte instruction. When using the assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

**Relative** - The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if, and only if, the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from - 126 to + 129 from the opcode address. The programmer need not worry about cal-

culating the correct offset if he uses the assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

**Indexed, no Offset** - In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

**Indexed, 8-bit Offset** - In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. This addressing mode is useful in selecting the kth element in an n element table. With this 2-byte instruction, k would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 (\$1FE is the last location at which the instruction may begin).

**Indexed, 16-bit Offset** - In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset except that this 3-byte instruction allows tables to be anywhere in memory. As with direct and extended, the assembler determines the shortest form of indexed addressing.

**Bit Set/clear** - In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single 2-byte instruction.

#### CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at \$004, \$005, \$006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port must be written using a single-store instruction.

**Bit Test and Branch** - The bit test and branch addressing mode is a combination of direct address-

ing and relative addressing. The bit which is to be tested and condition (set or clear) is included in the opcode, and the address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location. This single 3-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from -125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code registers.

#### CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at \$004, \$005, \$006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port must be written using a single-store instruction.

**Inherent** - In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as control instructions with no other arguments, are included in this mode. These instructions are one byte long.

#### INSTRUCTION SET

The EF6805U2 MCU has a set of 59 basic instructions, which when combined with the 10 addressing modes produce 207 usable opcodes. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

**Register/memory Instructions** - Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to table 1.

**Read-modify-write Instructions** - These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register; see Caution under Input/Output section. The test for negative or zero (TST) instruction is included in the read-modify-write instruction though it does not perform the write. Refer to table 2.

**Branch Instructions** - The Branch Instructions cause a branch from the program when a certain condition is met. Refer to table 3.

**Bit Manipulation Instructions** - The instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 4.

#### CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at \$004, \$005, \$006). A read operation on these registers is undefined.

Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port must be written using a single-store instruction.

**Control Instruction** - The control instructions control the MCU operations during program execution. Refer to table 5.

**Alphabetical Listing** - The complete instruction set is given in alphabetical order in table 6.

**Opcode Map** - Table 7 is an opcode map for the instruction used on the MCU.

Table 1 : Register/Memory Instructions.

Function	Addressing Modes																	
	Immediate			Direct			Extended			Indexed (no offset)			Indexed (8 bit offset)			Indexed (16 bit offset)		
	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Mnemonic	AG	2	2	R6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
Load A from Memory	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
Load X from Memory				B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
Store A in Memory				BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
Store X in Memory	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Add Memory to A	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
Add Memory and Carry to A	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
Subtract Memory	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
Subtract Memory from A with Borrow	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
AND Memory to A	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
OS Memory with A	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
Exclusive OR Memory with A	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
Arithmetic Compare A with Memory	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
Arithmetic Compare X with Memory	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
Bit Test Memory with A (logical compare)				BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
Jump Unconditional				BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9
Jump to Subroutine																		

Table 2 : Read-Modify-Write Instructions.

Function	Mnem	Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8 bit offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2'S complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

**Table 3 : Branch Instructions.**

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF interrupt mask bit is clear.	BMC	2C	2	4
Branch IFF interrupt mask bit is set.	BMS	2D	2	4
Branch IFF interrupt line is low.	BIL	2E	2	4
Branch IFF interrupt line is high.	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

**Table 4 : Bit Manipulation Instructions.**

Function	Mnemonic	Addressing Modes					
		Bit Set/clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF bit n is set.	BRSET n (n = 0.....7)				2 • n	3	10
Branch IFF bit n is clear.	BRCLR n (n = 0.....7)				01 + 2 • n	3	10
Set Bit n	BSET n (n = 0.....7)	10 + 2 • n	2	7			
Clear Bit n	BCLR n (n = 0.....7)	11 + 2 • n	2	7			



Table 5 : Control Instructions.

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2

Table 6 : Instruction Set.

Mnem	Addressing Modes										Condition Code				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (no offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			^	●	^	^	^
ADD		X	X	X		X	X	X			^	●	^	^	^
AND		X	X	X		X	X	X			●	●	^	^	●
ASL	X		X			X	X				●	●	^	^	^
ASR	X		X			X	X				●	●	^	^	^
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	^	^	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	^
BRSET										X	●	●	●	●	^
BSET									X		●	●	●	●	^
BSR					X						●	●	●	●	●
CLL	X										●	●	●	●	0

Condition Code Symbols :

- H Half Carry (from bit 3)
- I Interrupt Mask
- N Negative (sign bit)

Z

C

^

•

Zero

Carry/borrow

Test and Set if True, Cleared Otherwise

Not Affected

Table 6 : Instruction Set (continued).

Mnem	Addressing Modes									Condition Code					
	Inherent	Immediate	Direct	Extended	Relative	Indexed (no offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/clear	Bit Test & Branch	H	I	N	Z	C
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	^	^	^
COM	X		X			X	X				●	●	^	^	1
CPX		X	X	X		X	X	X			●	●	^	^	^
DEC	X		X			X	X				●	●	^	^	●
EOR		X	X	X		X	X	X			●	●	^	^	●
INC	X		X			X	X				●	●	^	^	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	^	^	●
LDX		X	X	X		X	X	X			●	●	^	^	●
LSL	X		X			X	X				●	●	^	^	^
LSR	X		X			X	X				●	●	0	^	^
NEQ	X		X			X	X				●	●	^	^	^
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	^	^	●
ROL	X		X			X	X				●	●	^	^	^
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	^	^	^
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	^	^	●
STX			X	X		X	X	X			●	●	^	^	●
SUB		X	X	X		X	X	X			●	●	^	^	^
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	^	^	●
TXA	X										●	●	●	●	●

Condition Code Symbols :  
 H Half Carry (from bit 3)  
 I Interrupt Mask  
 N Negative (sign bit)

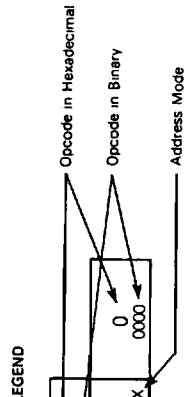
Z Zero  
 C Carry/borrow  
 ^ Test and Set if True, Cleared Otherwise  
 • Not Affected

## EF6805 HMOS FAMILY

Features	EF6805P2	EF6805P6	EF6805R2	EF6805R3	EF6805U2	EF6805U3
Technology	HMOS	HMOS	HMOS	HMOS	HMOS	HMOS
Number of Pins	28	28	40	40	40	40
On-chip RAM (bytes)	64	64	64	112	64	112
On-chip User ROM (bytes)	1100	1796	2048	3776	2048	3776
External Bus	None	None	None	None	None	None
Bidirectional I/O Lines	20	20	24	24	24	24
Unidirectional I/O Lines	None	None	6 Inputs	6 Inputs	8 Inputs	8 Inputs
Other I/O Features	Timer	Timer	Timer, A/D	Timer, A/D	Timer	Timer
External Interrupt Inputs	1	1	2	2	2	2
STOP and WAIT	No	No	No	No	No	No

Table 7 : 6805 HMOS Family Instruction Set Opcode Map.

Low	High	Bit Manipulation		Branch		Read-Modify-Write		Control		Register Memory		IX
0	1	BTB	BSC	DIR	BEL	INH	INH	INH	INH	DIR	EXT	IX
0	0000	0	0000	0	0000	0	0011	0	0000	0	0011	0
0	0001	1	BSET0	0	BRA	0	NEG	0	RTI	1	SUB	0
0	0010	0	BCLR0	1	BRN	1	NEG	1	RTS	2	SUB	1
0	0011	0	BSET1	0	BHI	0	COMA	0		3	SUB	2
0	0100	1	BCLR1	1	BLS	1	COMA	1	SWI	4	SUB	3
0	0101	0	BSET2	0	BCC	0	LSRA	0		5	CPX	0
0	0110	1	BCLR2	1	BCS	1	LSRA	1		6	CPX	1
0	0111	0	BSET3	0	BNE	0	RORA	0		7	SBC	0
0	1000	1	BCLR3	1	BEO	1	RORA	1		8	SBC	1
0	1001	0	BSET4	0	BHCC	0	ASRA	0		9	SBC	2
0	1010	1	BCLR4	1	BHCS	1	ASRA	1		0	CPX	0
0	1011	0	BSET5	0	BPL	0	LSLA	0		1	CPX	1
0	1100	1	BCLR5	1	BPL	1	LSLA	1		2	CPX	2
0	1101	0	BSET6	0	BIM	0	LSLA	0		3	CPX	3
0	1110	1	BCLR6	1	BIMC	1	LSLA	1		4	CPX	4
0	1111	0	BSET7	0	BIMTST	0	ROLA	0		5	CPX	5
0	1111	1	BCLR7	1	BIMTST	1	ROLA	1		6	CPX	6
1	0000	0	BSET0	0	BIMTST	0	ROLA	0		7	CPX	7
1	0001	1	BCLR0	1	BIMTST	1	ROLA	1		8	CPX	8
1	0010	0	BSET1	0	BIMTST	0	ROLA	0		9	CPX	9
1	0011	1	BCLR1	1	BIMTST	1	ROLA	1		0	CPX	0
1	0100	0	BSET2	0	BIMTST	0	ROLA	0		1	CPX	1
1	0101	1	BCLR2	1	BIMTST	1	ROLA	1		2	CPX	2
1	0110	0	BSET3	0	BIMTST	0	ROLA	0		3	CPX	3
1	0111	1	BCLR3	1	BIMTST	1	ROLA	1		4	CPX	4
1	1000	0	BSET4	0	BIMTST	0	ROLA	0		5	CPX	5
1	1001	1	BCLR4	1	BIMTST	1	ROLA	1		6	CPX	6
1	1010	0	BSET5	0	BIMTST	0	ROLA	0		7	CPX	7
1	1011	1	BCLR5	1	BIMTST	1	ROLA	1		8	CPX	8
1	1100	0	BSET6	0	BIMTST	0	ROLA	0		9	CPX	9
1	1101	1	BCLR6	1	BIMTST	1	ROLA	1		0	CPX	0
1	1110	0	BSET7	0	BIMTST	0	ROLA	0		1	CPX	1
1	1111	1	BCLR7	1	BIMTST	1	ROLA	1		2	CPX	2

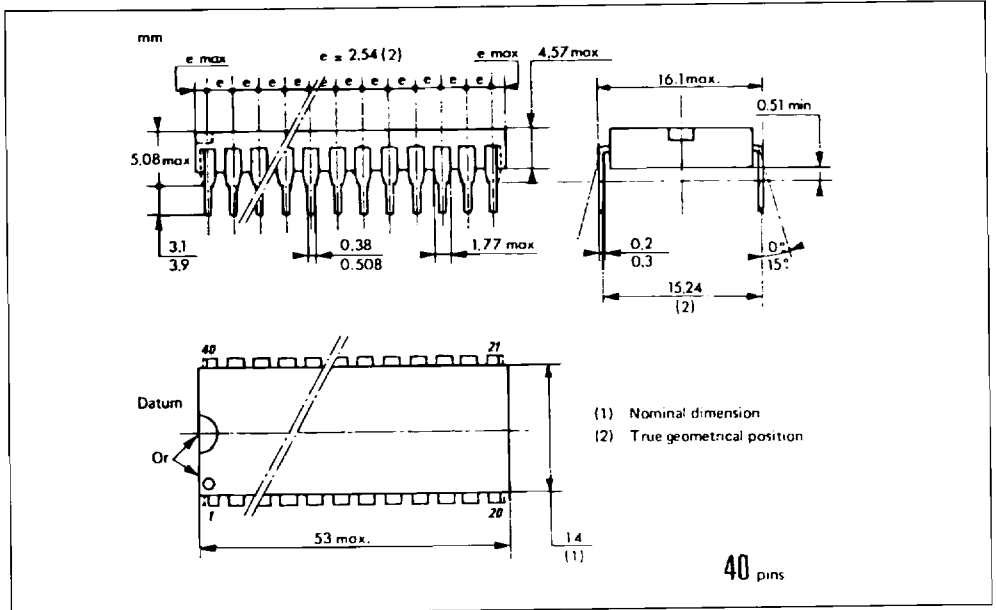


Abbreviations for Address Modes

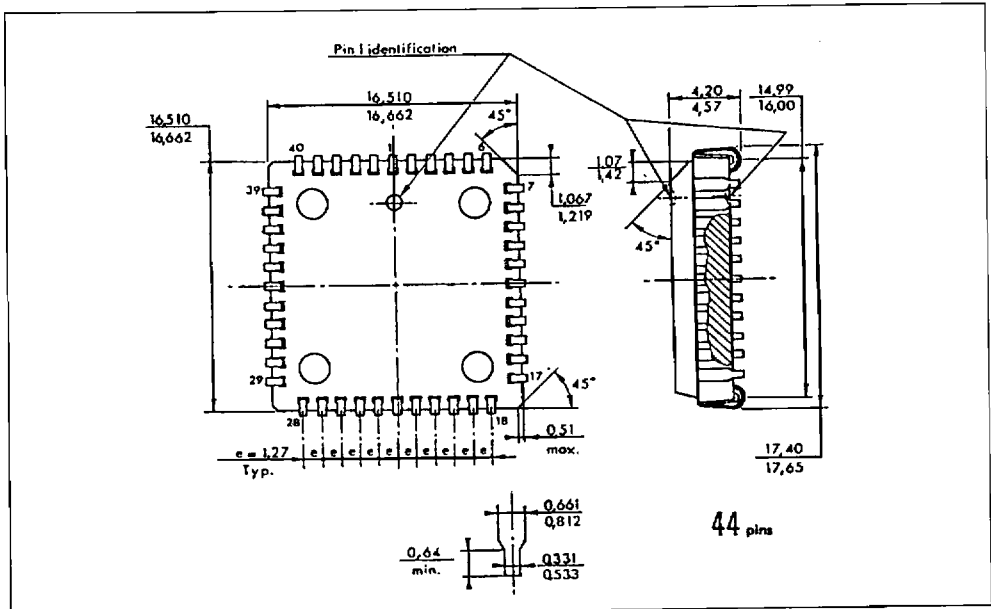
- INH Inherent
- IMM Immediate
- DIR Direct
- EXT Extended
- REL Relative
- BSC Bit Set/Clear
- BTB Bit Test and Branch
- IX Indexed (No Offset)
- IX1 Indexed, 1 Byte (8-Bit) Offset
- IX2 Indexed, 2 Byte (16-Bit) Offset

PACKAGE MECHANICAL DATA

CB-182 PLASTIC



CB-521



## ORDERING INFORMATION

The information required when ordering a custom MCU is listed below. The ROM program may be transmitted to SGS THOMSON on EPROM(s) or an EFDOS/MDOS\* disk file.

To initiate a ROM pattern for the MCU, it is necessary to first contact your local SGS-THOMSON representative or distributor.

### EPROMs

Two 2716 or one 2732 type EPROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The EPROM must be clearly marked to indicate which EPROM corresponds to which address space. The recommended marking procedure is illustrated below :

After the EPROM(s) are marked, they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

### VERIFICATION MEDIA

All original pattern media (EPROMs or floppy disk) are filled for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to SGS-THOMSON. The signed verification form constitutes the contractual agreement for creation of the customer mask. If desired, SGS THOMSON will program on blank EPROM from the data file used to create the custom mask and aid in the verification process.

### ROM VERIFICATION UNITS (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will

Whenever ordering a custom MCU is required, please contact your local SGS-THOMSON representative or SGS-THOMSON distributor and/or complete and send the attached "MCU customer ordering sheet" to your local SGS-THOMSON Microelectronics representative.

have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually unmarked, packaged in ceramic, and tested only at room temperature and 5 volts. These RVUs are included in the mask charge and are not production parts. The RVUs are thus not guaranteed by SGS THOMSON. Quality Assurance, and should be discarded after verification is completed.

### FLEXIBLE DISKS

The disk media submitted must be single-sided. EFDOS/MDOS\* compatible floppies.

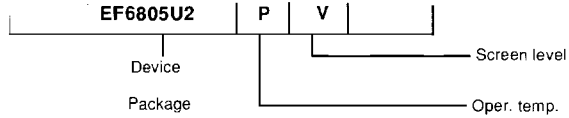
The customer must write the binary file name and company name on the disk with a felt-tip-pen. The minimum EFDOS/MDOS\* system files, as well as the absolute binary object file (Filename .LO type of file) from the 6805 cross assembler, must be on the disk. An object file made from a memory dump using the ROLLOUT command is also acceptable. Consider submitting a source listing as well as the following files : filename .LX (DEVICE/EXORciser loadable format) and filename .SA (ASCII Source Code). These files will of course be kept confidential and are used 1) to speed up the process in-house if any problems arise, and 2) to speed up the user-to-factory interface if the user finds any software errors and needs assistance quickly from SGS-THOMSON factory representatives.

EFDOS is SGS-THOMSON Disk Operating System available on development systems such as DEVICE...

MDOS\* is MOTOROLA's Disk Operating System available on development systems such as EXORciser...

\* Requires prior factory approval.

**ORDER CODES**



The table below horizontally shows all available suffix combinations for package, operating temperature and screening level. Other possibilities on request.

Device	Package					Oper. Temp			Screening Level			
	C	J	P	E	FN	L*	V	T	Std	D	G/B	B/B
EF6805U2			●		●	●	●	●	●	●		

**Examples :** EF6805U2P, EF6805U2FN, EF6805U2PV, EF6805U2FNV

**Package :** C : Ceramic DIL, J : Cerdip DIL, P : Plastic DIL, E : LCCC, FN : PLCC.  
**Oper. temp. :** L\* : 0°C to + 70°C, V : - 40°C to + 85°C, T : - 40°C to + 105°C, \* : may be omitted.  
**Screening level :** Std : (no-end suffix), D : NFC 96883 level D,  
 G/B : NFC 96883 level G, B/B : NFC 96883 level B and MIL-STD-883C level B.

EXORciser is a registered trademark of MOTOROLA Inc.



**EF6805 FAMILY - MCU CUSTOMER ORDERING SHEET**

Commercial reference :

Customer name : .....

Customer's marking :

Company : .....

Address : .....

Phone : .....

Application : .....

Specification reference ;

SGS-THOMSON Microelectronics reference

Special customer data reference\*

ROM capacity required :  bytes

Number of interrupt vector :

Temperature range :

- 0°C / + 70°C
- 40°C / + 85°C
- 40°C / + 105°C

Quality level :

- STD
- D
- Other\* (customer's quality specification ref.) :

Package

- Plastic
- PLCC

Software developed by :

- SGS-THOMSON Microelectronics application lab.
- External lab.
- Customer

**PATTERN MEDIA** (a listing may be supplied in addition for checking purpose) :

- EPROM Reference :
- EFDOS/MDOS\* disk file
  - 8" floppy
  - 5" 1/4 floppy
- Other \*

**OPTION LIST**

- Oscillator input
  - Xtal
  - RC
- Low voltage inhibit
  - Enabled
  - Disabled
- TTL
  - Port A output drive :
    - CMOS and TTL
  - Port C output drive :
    - TTL
- Timer clock source
  - Internal  $\phi$ 2 clock
  - Timer input pin
- Timer prescaler
 

<input type="checkbox"/> 1	<input type="checkbox"/> 4	<input type="checkbox"/> 16	<input type="checkbox"/> 64
<input type="checkbox"/> 2	<input type="checkbox"/> 8	<input type="checkbox"/> 32	<input type="checkbox"/> 128

\* Requires prior factory approval

Yearly quantity forecast :

- start of production date :
- for a shipment period of :

CUSTOMER CONTACT NAME

DATE :

SIGNATURE :

